Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2017**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Code :** | **14EC3053** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DESIGN OF SEMICONDUCTOR MEMORIES** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | Course  Outcome | Marks |
| 1. | a. | With neat diagram explain the operation of a 3T and 1T DRAM cell. | CO2 | 8 |
| b. | Differentiate between hard error and soft error and discuss how soft error occurs in DRAM. | CO1 | 12 |
| (OR) | | | | |
| 2. | a. | Expand SRAM and justify why it is called so. | CO1 | 4 |
| b. | List the advantages of SOI technology over bulk silicon technology in the design of RAM. | CO1 | 4 |
| c. | Describe with necessary diagrams, different types of application specific SRAM. | CO1 | 12 |
| 3. | a. | Justify the usage of trench capacitor in the design of high density DRAM. | CO1 | 5 |
|  | b. | With neat diagram explain the read, write operation of a conventional SRAM cell and the operation of its peripheral circuits - write circuitry and sense amplifier. | CO2 | 15 |
| (OR) | | | | |
| 4. | a. | Justify that DRAM is used in Main memory. | CO1 | 5 |
|  | b. | Describe with necessary diagrams, different types of application specific DRAM. | CO1 | 15 |
| 5. | a. | Justify the need for OTP EPROM | CO1 | 4 |
|  | b. | With state diagram, indicate how a 0 to 1 transition fault occur in a memory cell | CO3 | 4 |
|  | c. | Indicate different memory cell design of PROM and explain how the cells are programmed. | CO2 | 12 |
| (OR) | | | | |
| 6. | a. | Discuss about the reliability issues of EEPROM and Flash memory. | CO2 | 10 |
|  | b. | With suitable figures, explain how program, read and erase operations are performed in a Flash memory. | CO2 | 10 |
| 7. | a. | Define Fowler-Nordheim tunneling mechanism. | CO1 | 4 |
|  | b. | Compare the state transition diagrams of 2 cells in fault free and faulty state assuming the fault to be inversion coupling fault when the aggressor moves from 1 to 0. | CO3 | 16 |
| (OR) | | | | |
| 8. | a. | Draw the state transition diagram of 2 memory cells in fault free case. | CO3 | 4 |
|  | b. | Discuss about various Functional Testing Algorithms. | CO2 | 16 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Compare the usage of FRAM and EEPROM in nonvolatile memory applications. | CO3 | 4 |
|  | b. | With neat diagram of FRAM hysteresis curve explain the polarization effect, FRAM cell and memory operation. | CO2 | 16 |

ALL THE BEST